What is claimed is:

1. A single crystal silicon wafer having a central axis, a front side and a back side which are generally perpendicular to the central axis, a central plane between the front and back sides, a circumferential edge, and a radius extending from the central axis to the circumferential edge, the wafer comprising:

a first axially symmetric region, extending radially inwardly from the circumferential edge, in which silicon self-interstitials are the predominant intrinsic point defect and which is substantially free of agglomerated interstitial defects; and,

a second axially symmetric region in which vacancies are the predominant intrinsic point defect, the second axially symmetric region comprising a surface layer extending from the front side toward the central plane and a bulk layer extending from the surface layer to the central plane, the number density of agglomerated vacancy defects present in the surface layer being less than the concentration in the bulk layer.

2. The wafer as set forth in claim 1 wherein the surface layer has a depth, as measured from the front side toward the central plane, of at least about 2 microns.

3. The wafer as set forth in claim 1 wherein the surface layer has a depth, as measured from the front side toward the central plane, of at least about 4 microns.

4. The wafer as set forth in claim 1 wherein the surface layer has a depth, as measured from the front side toward the central plane, of at least about 8 microns.

5. The wafer as set forth in claim 1 wherein the surface layer has a depth, as measured from the front side toward the central plane, of at least about 10 microns.

6. The wafer as set forth in claim 1 wherein the second axially symmetric region has a width, as measured radially from the central axis toward the circumferential edge, which is at least about 25% of the length of the radius.

7. The wafer as set forth in claim 1 wherein the second axially symmetric region has a width, as measured radially from the central axis toward the circumferential edge, which is at least about 50% of the length of the radius.

8. The wafer as set forth claim 1 wherein the wafer has an oxygen content which is less than about 13 PPMA.

9. The wafer as set forth in claim 1 wherein the first axially symmetric region has a width, as measured from the circumferential edge radially toward the center axis, which is at least about 10% the length of the radius.

10. The wafer as set forth in claim 1 wherein the first axially symmetric region has a width, as measured from the circumferential edge radially toward the center axis, which is at least about 30% the length of the radius.

11. The wafer as set forth in claim 1 wherein the first axially symmetric region has a width, as measured from the circumferential edge radially toward the center axis, which is at least about 60% the length of the radius.

12. The wafer as set forth in claim 1 wherein the first axially symmetric region has a width, as measured from the circumferential edge radially toward the center axis, which is at least about 80% the length of the radius.

13. The wafer as set forth in claim 1 wherein the number density of agglomerated vacancy defects present in the surface layer is about 20% less the number density of the bulk layer.

14. The wafer as set forth in claim 1 wherein the number density of agglomerated vacancy defects present in the surface layer is about 40% less the number density of the bulk layer.

15. The wafer as set forth in claim 1 wherein the number density of agglomerated vacancy defects present in the surface layer is about 80% less the number density of the bulk layer.

16. The wafer as set forth in claim 1 wherein the surface layer is substantially free of agglomerated intrinsic point defects.

17. The wafer as set forth in claim 1 wherein the wafer has a diameter of at least about 150 mm.

18. The wafer as set forth in claim 1 wherein the wafer has a diameter of at least about 200 mm.

19. A process for preparing a single crystal silicon wafer which is substantially free of agglomerated intrinsic point defects, the process comprising thermally annealing a single crystal silicon wafer at a temperature in excess of about 1000°C in an atmosphere of hydrogen, argon or a mixture thereof, said wafer having a central axis, a front side and a back side which are generally perpendicular to the central axis, a central plane between the front and back sides, a circumferential edge, a radius extending from the central axis to the circumferential edge, a first axially symmetric region extending radially inward from the circumferential edge in which silicon self-interstitials are the predominant intrinsic point defect and which is substantially free of agglomerated interstitial defects, and a second axially symmetric region, located radially inward of the first axially symmetric region, in which vacancies are the predominant intrinsic point defect, the thermal anneal acting to dissolve agglomerated vacancy defects present in the second axially symmetric region within a layer extending from the front side toward the central plane.

20. The process as set forth in claim 19 wherein the wafer is thermally annealed in an argon atmosphere.

21. The process as set forth in claim 19 wherein the wafer is thermally annealed by heating the wafer to a temperature ranging from about 1100 to about 1300°C.

22. The process as set forth in claim 21 wherein the wafer is thermally annealed for about 1 to about 4 hours.

23. The process as set forth in claim 19 wherein the wafer is thermally annealed by heating the wafer to a temperature ranging from about 1200 to about 1250°C.

24. The process as set forth in claim 23 wherein the wafer is thermally annealed for about 2 to about 3 hours.

25. The process as set forth in claim 19 wherein the layer extends from the front side and toward the central plane to a depth of about 4 microns.

26. The process as set forth in claim 19 wherein the layer extends from the front side and towards the central plane to a depth of about 8 microns.

27. The process as set forth in claim 19 wherein the layer extends from the front side and towards the central plane to a depth of about 10 microns.

28. The process as set forth in claim 19 wherein the layer extends from the front side and towards the central plane to a depth of about 20 microns.

29. The process as set forth in claim 19 wherein the first axially symmetric region has a width, as measured from the circumferential edge radially toward the center axis, which is at least about 10% the length of the radius.

30. The process as set forth in claim 19 wherein the first axially symmetric region has a width, as measured from the circumferential edge radially toward the center axis, which is at least about 30% the length of the radius.

31. The process as set forth in claim 19 wherein the first axially symmetric region has a width, as measured from the circumferential edge radially toward the center axis, which is at least about 60% the length of the radius.

32. The process as set forth in claim 19 wherein the first axially symmetric region has a width, as measured from the circumferential edge radially toward the center axis, which is at least about 80% the length of the radius.

33. The process as set forth in claim 19 wherein the wafer has a diameter of at least about 150 mm.

34. The process as set forth in claim 19 wherein the wafer has a diameter of at least about 200 mm.

35. A process for preparing a silicon wafer which is substantially free of agglomerated intrinsic point defects, the wafer being sliced from a single crystal silicon ingot having a central axis, a seed-cone, an end-cone, and a constant diameter portion which extends between the seed-cone and the end-cone, the constant diameter portion having a circumferential edge and a radius extending from the circumferential edge toward the central axis, the ingot being grown from a silicon melt and then cooled from the solidification temperature in accordance with the Czochralski method, the process comprising:

growing the single crystal silicon ingot, wherein the growth velocity, v, and an average axial temperature gradient, G_0, are controlled during the growth of the constant diameter portion of the ingot over a temperature range from solidification to a temperature of no less than about 1325 °C to cause the formation of a segment of the constant diameter portion which, upon cooling of the ingot from the solidification temperature, comprises a first axially symmetrical region extending radially inward from the circumferential edge toward the central axis in which silicon self-interstitials are the predominant intrinsic point defect and which is substantially free of agglomerated interstitial defects, and a second axially symmetric region in which vacancies are the predominant intrinsic point defect;

slicing the segment of the constant diameter portion to obtain a wafer, the wafer having a front side and a

back side which are generally perpendicular to the central axis, and a central plane between the front and back sides, the wafer comprising the first and second axially symmetric regions; and,

thermally annealing the wafer at a temperature in excess of about 1000°C in an atmosphere of hydrogen, argon, oxygen, nitrogen, or a mixture thereof to dissolve agglomerated vacancy defects present in the second axially symmetric region within a layer extending from the front surface toward the central plane of the wafer.

36. The process as set forth in claim 35 wherein the wafer is thermally annealed in an argon atmosphere.

37. The process as set forth in claim 35 wherein the wafer is thermally annealed by heating the wafer to a temperature ranging from about 1100 to about 1300°C.

38. The process as set forth in claim 37 wherein the wafer is thermally annealed for about 1 to about 4 hours.

39. The process as set forth in claim 35 wherein the layer extends from the front side and toward the central plane to a depth of at least about 4 microns.

40. The process as set forth in claim 35 wherein the first axially symmetric region has a width, as measured from the circumferential edge radially toward the center axis, which is at least about 60% the length of the radius.